MCM Packaging for Present- and Next-Generation High Clock-Rate Digital- and Mixed-Signal Electronic Systems: Areas for Development

Barry K. Gilbert, *Senior Member, IEEE,* and Guang-Wen (George) Pan, *Senior Member, IEEE*

(Review Paper)

***Abstract*— This paper will review the manner in which electronic packaging will be driven by the high-level performance requirements of next-generation mixed-signal systems, and by the evolving characteristics of next-generation integrated circuits. Present performance and fabrication limitations of the multichip module (MCM) technology will be discussed, as well as possible approaches to remove or minimize these constraints. Areas fruitful for research by the simulation community will be noted. This review is intended to provide a broad applications-oriented framework for the theoretical and simulation-directed papers in this special issue on interconnect and packaging.**

***Index Terms*— AID converters, digital receivers, digital-signal processors, electromagnetic modeling, multichip modules, S-parameters.**

I. Introduction

THIS special issue of IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES is featuring current research into simulation approaches for advanced electronic packaging, such as the still-emerging technology of multichip modules (MCM's), which are now available from a number of vendors and manufactured with a variety of different fabrication recipes. This paper will provide a frame of reference for, and a tutorial introduction to, the algorithmic and simulation work discussed throughout this special issue, and will provide an update to the simulation community on the difficulties confronted by the systems designers who wish to employ the MCM's and the vendors who must find ways to fabricate these structures. This paper will: 1) survey the state of the art of the electronic packaging technology in terms of the commercial and military applications in which they are being employed; 2) describe the strengths and weaknesses of the MCM's from the users' and the fabricators' point of view; 3) describe fruitful areas for research at the materials and processing level; and 4) offer suggestions for ways in which the simulation and modeling community can assist in the evolution of the overall packaging technology.

These discussions will concentrate solely on MCM development, since the related printed wiring board (PWB) technology is considered mature. However, several comments regarding simulation requirements do apply to the PWB technologies as well. We define MCM's as multilayer sandwiches of dielectric and conducting layers, on which integrated circuits ("chips") and passive components (if any) are mounted directly on (or inside of) the sandwich structure, without separate packaging for each of the active components. That is, the chips are mounted "bare" onto the MCM's, which then provide the required power and ground, as well as all the signal interconnect and the electrical interface to the external environment. The entire MCM, including chips and passive components, may be placed in a hermetic package much like a large single-chip carrier, or may be directly covered with a sealant material (such as epoxy or a glass passivation coating) to protect the components from physical damage.

Three general categories of MCM's will be mentioned repeatedly.

1) *Laminate MCM's (MCM-L's)*: are manufactured through the lamination of sheet layers of organic dielectric, and are very similar to traditional printed circuit board technology; in fact, the dielectric layers and the interconnects are developed in much the same way as for laminated printed circuit boards [1]. The line geometries and via diameters are typically half or less the size of those found in traditional circuit boards. As will be discussed later in this paper, these MCM's exhibit very low line losses up to relatively high frequencies because the lines are thick and wide; however, the vias are typically quite tall and also much wider than the lines, thus causing substantial impedance discontinuities and wavefront reflections for frequency components above 500 MHz.
2) *Ceramic MCM's (MCM-C's)*: are manufactured by stacking unfired layers of ceramic dielectric (i.e., in their flexible, unfired state), onto which liquid metal lines are "silk screened" using a metal ink process. The individual inked layers are then aligned, pressed together, and "cofired" at 800–900 °C, or 1500–1600 °C

Manuscript received January 10, 1997; revised June 5, 1997. This work was supported in part by the Electronics Technology Office of the Defense Advanced Research Projects Agency (DARPA/ETO), through Contract N66001-94-C-0051 from NCCOSC/NRaD.

B. K. Gilbert is with the Special Purpose Processor Development Group, Mayo Foundation, Rochester, MN 55905 USA.

G.-W. Pan is with the Department of Electrical and Computer Engineering, Arizona State University, Tempe, AZ 85287 USA.

Publisher Item Identifier S 0018-9480(97)07402-4.

(depending on the composition of the ceramic material) into a solid planar structure, onto which integrated circuits can be installed [2]. These MCM's can, if fabricated with excellent dimensional tolerance control, exhibit low line losses for the same reasons as for the MCM-L's. Unfortunately, as will be discussed later, like the MCM-L's, their vias are also tall and wide, resulting in substantial impedance discontinuities and wavefront reflections for frequency components above 500 MHz.

3) *Deposited MCM's (MCM-D's)*: are manufactured through the deposition of organic or inorganic [3] dielectrics onto a silicon or alumina support substrate. After each dielectric layer is deposited, one of several techniques is used to pattern metal lines as well as metal "vias" which penetrate the dielectric layers to connect adjacent metal layers [3], [4]. The chips are then installed on the upper surface, and attached electrically through wire bonds or other means such as tape automated bond structures, or even by mounting the chips face down on the surface, with metal balls serving as the electrical connections between the chip and matching pads on the MCM's. As will be discussed in detail later, the MCM-D line cross sections are typically smaller than for MCM-C's or MCM-L's, resulting in higher resistive line losses; however, their via heights are typically quite small, and their via cross sections are equivalent to the linewidths, resulting in low levels of impedance discontinuity and wavefront reflections, in comparison to the MCM-L's and MCM-C's.

The variations (recipes) for the manufacture of MCM's which have been reported are almost endless, and include "chips-first" structures [4]–[5], in which the chips are actually buried within the laminate; "chips-last" (described above), in which the chips are mounted directly on the upper surface of the laminate [6]; MCM-D/L, in which the lower layers are laminated, but the upper layers are deposited, and so on. The following discussion will attempt to remain generic, unless there is a specific reason to mention a particular fabrication recipe.

II. Present Commercial Applications of MCM'S

During the past decade a considerable struggle has occurred to launch the new MCM packaging technology, including the financial failure of a number of companies with potentially excellent technology, but insufficient cash flow to continue operations because of the slow buildup of business. Now, however, several stable manufacturing operations have emerged, offering products employing all of the major types of MCM's. As is the case for integrated circuits, the commercial world is driving the volume production applications for MCM's, while the U.S. military is driving the most technically sophisticated applications for MCM's.

Commercial applications have to the present been concentrated in "core" microprocessors, including the microprocessor itself, the Level 2 (L2) cache, and occasionally a bus controller as well. Alternately, specialized controller functions using application-specific integrated circuits (ASIC's) are also finding their way into MCM's (Fig. 1). One company, using inorganic chips-last MCM's, has designed and manufactured several generations of a complete UNIX-based microprocessor small enough to be employed in lap-top computers—tens of thousands of these units have been manufactured. Several other large consumer electronics companies are known to be developing similar products. These all-digital modules are designed to operate at clock rates of 100–200 MHz, a moderately high clock rate for the consumer electronics world, but as will be made clear later, a relatively slow rate compared to a number of the evolving military applications.

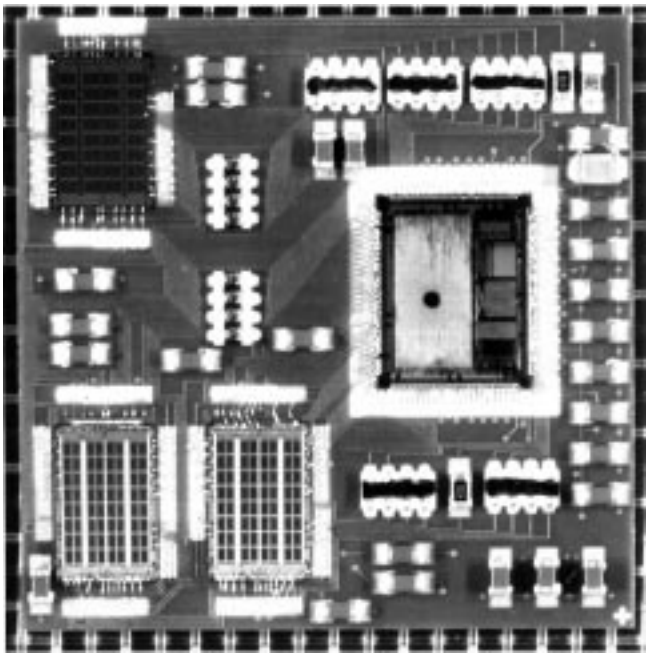

Fig. 1. Photograph of specialized controller MCM for a consumer electronics product. Note, in addition to the four active integrated circuits, the large number of discrete resistors and capacitors installed on the surface of this seven-layer MCM-L. The MCM-L is typically covered with an epoxy overcoat, and solder attached to a motherboard using ball grid-array technology. (14433)

Many of the commercial microprocessors themselves operate at much higher clock rates on-chip than the system boards onto which they are mounted (the chips contain a phase-locked loop to count up the clock rate fed to them from the system board); the consumer electronics manufacturers have been reluctant to operate their system boards at the microprocessor clock rates because of bandwidth limitations of large PWB's at elevated clock rates. The MCM technologies can easily support these higher clock rates, but the prior negative experiences have resulted in the view (though incorrect) that board-level clock rates cannot exceed 100 MHz. The frequency regime between 100–500 MHz is a good one for MCM's if the consumer companies can traverse the learning curve to allow proper exploitation of the technology. No automotive applications for MCM's have emerged at the time of this writing, but can be expected within the next few years.

The second significant area of development in the consumer market is for systems which combine both digital and analog integrated circuits on the same MCM, particularly for cellular telephones and pagers. Such systems are referred to

as "mixed-signal" or "mixed mode" systems, because of the combined analog and digital content. Because the designers of such systems are extremely cost conscious, manufacturing costs drive this market totally, in spite of the fact that the modules themselves must operate well at center frequencies of 900 MHz (in the United States) to 2.5 GHz (in Europe and the Far East). These systems are designed to tolerate wide ranges in MCM and component tolerances, so that the assembled modules will work, regardless of the quality of the individual components. To minimize manufacturing costs, the less precise but least costly MCM-L's (which, after all, are an evolutionary step from the PWB technology) are increasingly being manufactured within large panels, and are then separated from one another by sawing or snapping the MCM's from the panels. Panelized MCM's are intended to be run in fabrication lots of 10 000–100 000 units per month. All commercial MCM vendors seek such business in preference to smaller run MCM's requiring higher levels of manufacturing precision, for both cost and profit reasons.

III. Present Military Applications of MCM'S

The U.S. military has envisioned many uses for all of the MCM technologies, for completely digital systems and also for very complex mixed-signal systems. As will be noted below, the level of technical sophistication of the military requirements far exceeds that of the most aggressive commercial applications. However, the required manufacturing volumes are extremely small, in the view of the MCM fabricators: a fabrication run of a few thousand units to satisfy the total requirements of a military system is simply not attractive financially, in comparison to much larger production runs for commercial or consumer applications. This situation places the military, which could propel the state of the MCM art, in the disadvantageous position of having little or no access to the manufacturing facilities which they require. A project sponsored by the Defense Advanced Research Projects Agency (DARPA) over the past few years to provide low-volume manufacturing access to high-volume manufacturing lines has not succeeded. Because this problem could jeopardize the success of a number of future Department of Defense (DOD) projects, it is presently being revisited by DARPA; another type of solution for low-volume, precision MCM manufacturing is presently being developed.

The list of electronic systems which the DOD is considering for implementation (and particularly miniaturization) using MCM's is extremely broad, and includes all of the military services. A few examples which the DOD is investigating include:

1) "universal" handheld radios for special forces and conventional ground troops which can communicate with a variety of older radios employing different transmission protocols;
2) a complex communications system, essentially a combination of a telephone exchange and a multifrequency radio transceiver, made sufficiently light and compact that it will fit into the payload bay of a high altitude unmanned air vehicle (UAV)—which is then positioned over a battlefield to give friendly forces unprecedented communications capability;
3) complete navigation, communication, and sensor packages for very small UAV's, with much less carrying capacity than any earlier UAVs;
4) much of the processing electronics for next-generation combat aircraft such as the F-22 and Joint Strike Fighter;
5) next-generation radar, communications, and electronic warfare (EW) receivers, which employ analog-to-digital (A/D) converters and digital-to-analog (D/A) converters operating in the gigahertz range to convert analog signals to digital sample streams immediately behind their receiving antennas, and thereafter, process the incoming information streams using modern digital signal processing techniques.

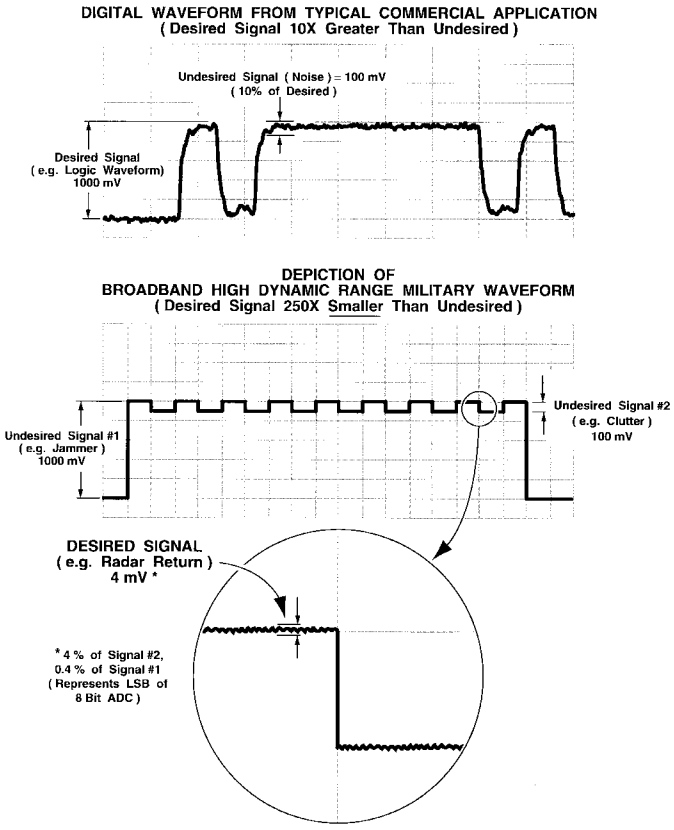

Fig. 2. Conceptual illustration of time-domain waveform purity needed for broad-band high dynamic-range military systems relying on high-performance A/D converters, in contradistinction to less stringent waveform-conformation requirements of conventional digital systems. (14599)

A brief review of the requirements of number 4 above—the emerging family of all-digital receivers—is a good example of the performance capabilities which will be required of future electronic packaging. The "front ends" of the emerging family of all-digital receivers consists of an analog noise shaping filter with a high quality factor (Q), a low noise amplifier (LNA) to establish the noise figure of the system (at the minimum possible value), an A/D converter to digitize the incoming information at rates of 3–6 gigasamples/s (presently) to 25 gigasamples/s (within the next few years), and a digital demultiplexer and first-stage digital-signal processor to decrease the effective data rates. The "front" of the front

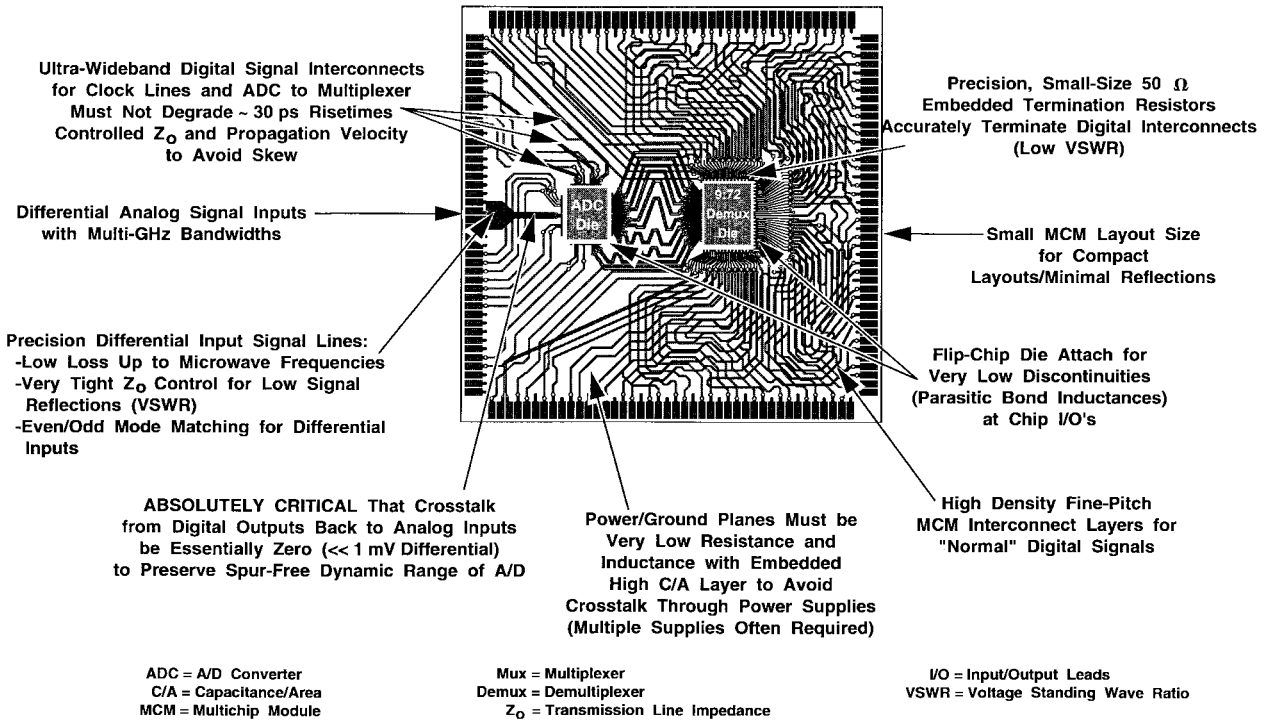

Fig. 3. Requirements for precision MCM's in support of next-generation all-digital receivers. Specific requirements are with reference to an actual digital receiver MCM (actual layout artwork shown) designed to accept a 3-gigasample/s 8-bit A/D converter and matching 9:72 demultiplexer chip. (14588)

end of these receivers places the strictest requirements on the packaging, because the A/D converters must digitize the incoming signal to a very high degree of accuracy. In these systems, the signal of interest is buried far beneath the background noise; for example, the amplitude of the radar return from a small sea-skimming cruise missile is much less than the false return from the sea surface itself (referred to as the "clutter"). This conceptual relationship between noise amplitudes in digital systems and in mixed-signal systems is illustrated diagrammatically in Fig. 2.

A number of signal processing "tricks" can be used to recover a signal buried in noise, but only if the antenna output has been digitized faithfully enough that the desired signal still remains, accurately reproduced by the A/D converter. Signal conversion fidelity levels of 60–70 dB, or even more, between the largest and smallest amplitude signal must be preserved. This level of fidelity in turn requires that the interconnects between the bandlimiting filter, the LNA, and the A/D converter not contaminate the input signal with reflections or standing waves over the entire input frequency band, and not contribute distortion or feedback signal from the outputs to the inputs directly or through the power supply pin's on the A/D converter chip (i.e., through inadequate power and ground supplies). Similar constraints are necessary for D/A converters used in direct digital synthesizers to generate pure sine waves for a variety of synthesized waveform systems such as all digital radios. Finally, all-digital output bits from an A/D converter system must often be timed to emerge from the A/D subsystem with very little phase skew. Fig. 3 incorporates a photo of the signal-layer artwork (for clarity; power and ground layers are not shown) for such an MCM which performs this task for an 8-bit 3-GHz A/D converter developed for an experimental Navy radar system [7]. The design and fabrication of an MCM to support such subsystems is complex, and as in the MCM of Fig. 3, does not always achieve all of the performance goals, due to limitations in the supporting technologies for MCM's.

IV. Technical Limitations of Present MCM Technology

The difficulty in achieving these new capabilities, from the viewpoint of proposed military systems, is that after a decade of very active support of the MCM industry by the DOD, the total resources of the MCM fabrication industry are directed to the production of modules for the commercial and consumer electronics markets, with very minimal performance standards. In many cases the MCM vendors do not clearly understand the limits of their own processes. Manufacturing tolerances are very loose, apparently since digital and cellular-phone designs are developed to survive very poor component tolerances. Our findings in this regard over the past decade, working with two dozen vendors of MCM-L's, MCM-C's, and MCM-D's, are illustrative of the issues remaining to be addressed.

Impedance control in the majority of MCM's is very minimal. Fig. 4 illustrates the results of testing a very large number of 50-Ω transmission lines on MCM's of the three major types. Since the standard deviations are very large, two different MCM's from the same fabrication run may have different line impedances by as much as 12–14 Ω, and still be within one standard deviation of the mean. The apparently small standard deviation (tight grouping) of line impedances for the MCM-C in the lower right panel of Fig. 4

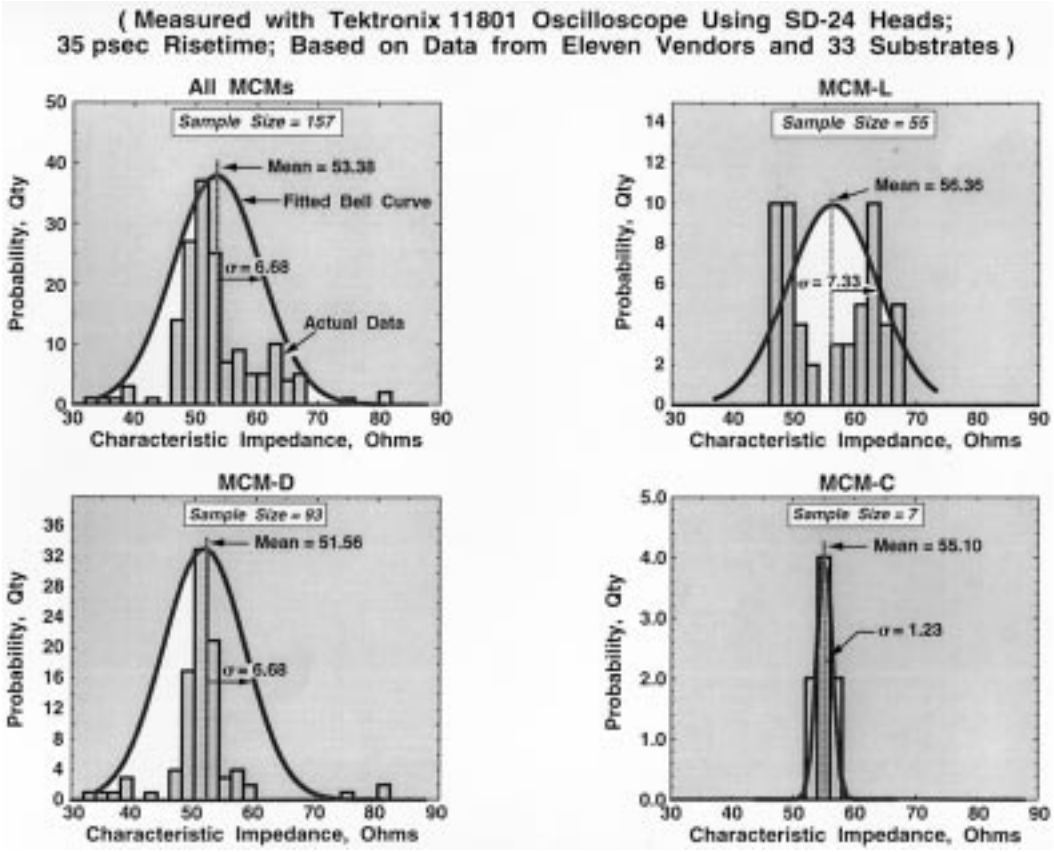

Fig. 4. Combined characteristic impedance distribution of nominal 50-Ω microstrip and stripline transmission lines in three types of MCM's. The apparent tight grouping of the MCM-C structures is an artifact of the small number of structures measured in these substrates. Note considerable deviation of the mean impedances from 50 Ω and the large value of standard deviation in all MCM types. (14609)

is an atypical result caused by the fact that all seven lines measured were from a single coupon; even in these structures, the mean impedance was 55.1 Ω rather than 50 Ω. Further, the line *resistances* were unacceptably high because the line cross sections were very small, as will be discussed below. (Note that the 50-Ω impedance value is not sacred; on-MCM transmission lines can be adjusted for other impedance values such as 68 or 75 Ω if more convenient. We selected 50 Ω for the test lines measured here because it matches well with commercially available microwave test equipment. The errors in achieving the target line impedance, and tight statistical control, depicted in Fig. 4 with a 50-Ω target, would be expected to occur at other line impedances as well.) Because many of the wide bandwidth or high center frequency (or high clock rate) military systems require a terminated transmission line environment, these wide variations make it impossible to choose termination network values with any assurance that they will match the line impedances; in turn, virtually guaranteeing that standing waves will appear at one or more locations along the input signal path between the filter, LNA, and A/D converter input.

When we employ microwave performance criteria for the interconnects by measuring carefully designed microwave test structures on a large number of MCM's, we find that these criteria confirm the poor control of fabricated parameters at all levels of the process. Insertion loss, S_{21}, a measure of the amount of signal energy which reaches the far end of a line over a range of frequencies, should be as close as possible to 0 dB across the passband of interest to assure that all signal energy reaches its destination at the far end of each interconnect. Fig. 5 shows measured levels of S_{21} for 5-mm striplines on a large number of test structures fabricated in both MCM-L and organic MCM-D technologies. Note the wide variability between different samples, and the high loss levels. Conversely, simulations show that these losses

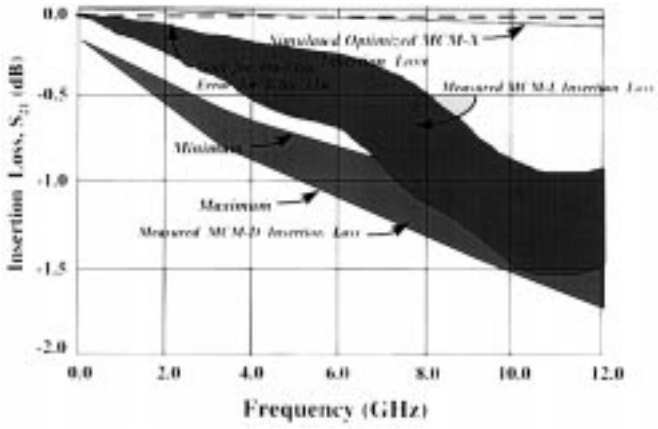

Fig. 5. Measured maximum and minimum insertion loss of 5-mm stripline transmission lines on large numbers of MCM-L and MCM-D test structures. Simulated losses on optimized "MCM-X" structure indicate that improved fabrication techniques can significantly decrease these losses. The loss goal for 8-bit A/D converters is also indicated. (14553)

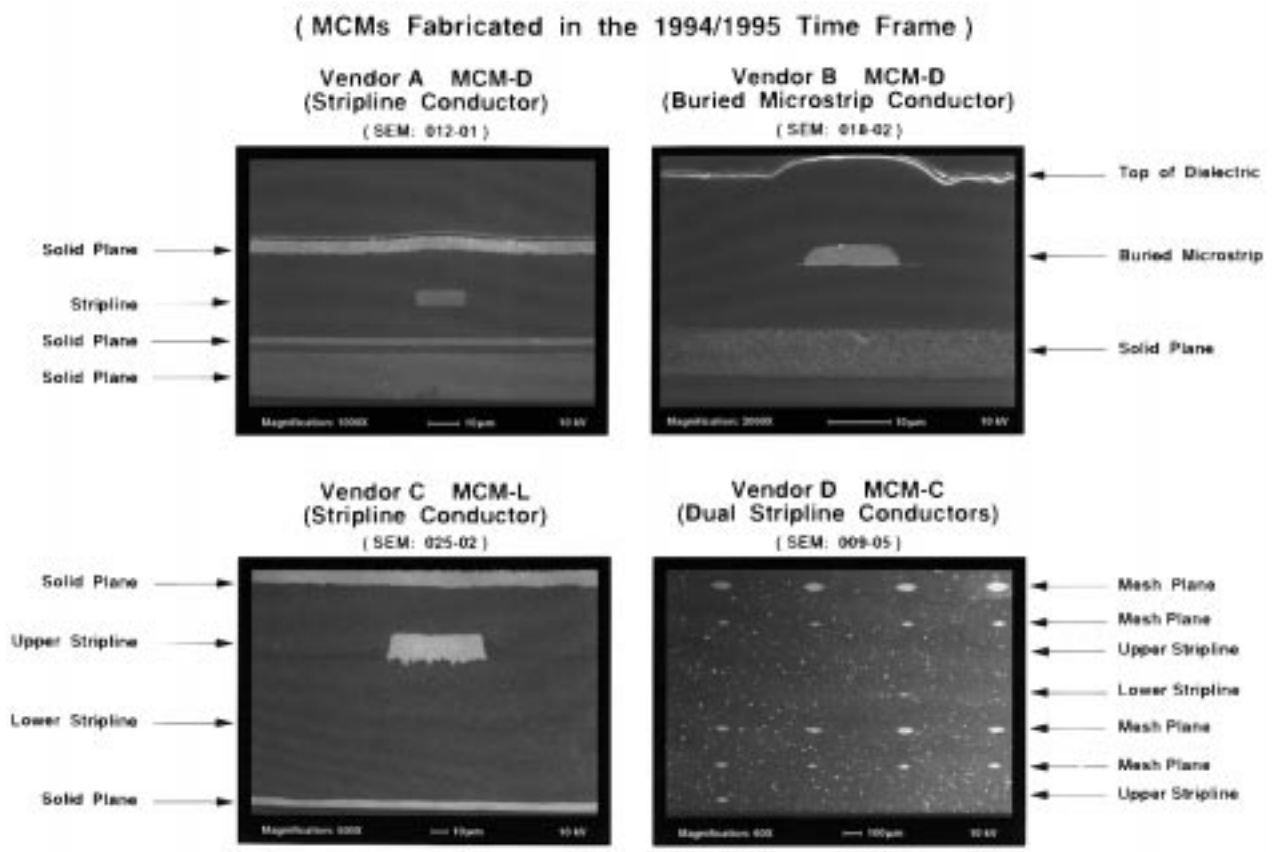

Fig. 6. Scanning electron micrographs of typical interconnects in MCM-D's, MCM-L's, and MCM-C's manufactured with different fabrication recipes. Note the considerable variation from ideal rectangular cross section typical of most of the lines. Only Vendor A's lines have a truly rectangular cross section, and will behave well at high frequencies and "track" the EM models for these lines. Note "ears" and nonuniform cross sections in Vendor B's lines; roughness in Vendor C's lines, which cause serious skin-effect problems; tiny cross sections of Vendor D's lines. (14523)

can be substantially reduced: Fig. 5 depicts simulated S_{21} losses in a hypothetical "MCM-X" technology, which was postulated as a feasible extension of conventional organic MCM-D processes presently in existence, simply by modifying a number of fabrication parameters such as linewidth, line thickness, sheet resistance of the as-deposited metal, etc., each by a few tens of percentage points (i.e., no "heroic" values were assumed, only minor improvements across a number of fabrication parameters). Note that S_{21} losses in this "MCM-X" technology are substantially better than the as-measured values. We believe that these improved parameters are achievable with improved fabrication methods.

The primary causes of some of these problems can be clearly observed by cross sectioning the MCM structures. Fig. 6 clearly shows that the lines are not rectangles or even trapezoids; they have a wide range of shapes, which in turn creates two problems: first, the lines do not measure as they simulate because the simulations usually assume rectangular or trapezoidal cross sections (in fact, the line cross sections in the MCM-C structures in the lower right panel were so small as to be barely visible). Second, the uneven surfaces created by the rough line structures make it difficult to fabricate more than a few metal layers, since the uppermost layers are so nonplanar that it becomes impossible to apply subsequent layers of dielectric or metal as the structures are built up. Similarly, via structures as fabricated are vastly different from those typically assumed in simulation models, as may be observed in Fig. 7.

The wire bonds used to provide electrical connections between the MCM interconnects and the chip pads are also sites for loss of signal integrity, as illustrated in the upper panels of Fig. 8 for both MCM-L's and MCM-C's. The panels of Fig. 8 compare the effects of wire bonds of different lengths with so-called flip-chip attachment approaches, which allow direct contact between the chip pads and matching pads on the MCM's. As may be observed, the flip-chip attachment typically displays the smallest S_{21} losses over any given passband. Conversely, the wire-bond attachments show large variations, particularly for frequency components greater than 4 GHz. The lower panels of Fig. 8 depict return loss, S_{11}, the amount of energy reflected back at the source. Most discussions in the literature concentrate on S_{21} effects, because on first review they appear to be the most important. However, to assure a minimum amount of standing waves on an interconnect, and hence, the most uniform behavior across a wide range of frequencies, S_{11} should be less than -20 dB across the entire passband of interest. Here again, wire bonds of all lengths perform at a significantly inferior level in comparison to flip-chip attachment for all frequency components above a few hundred MHz.

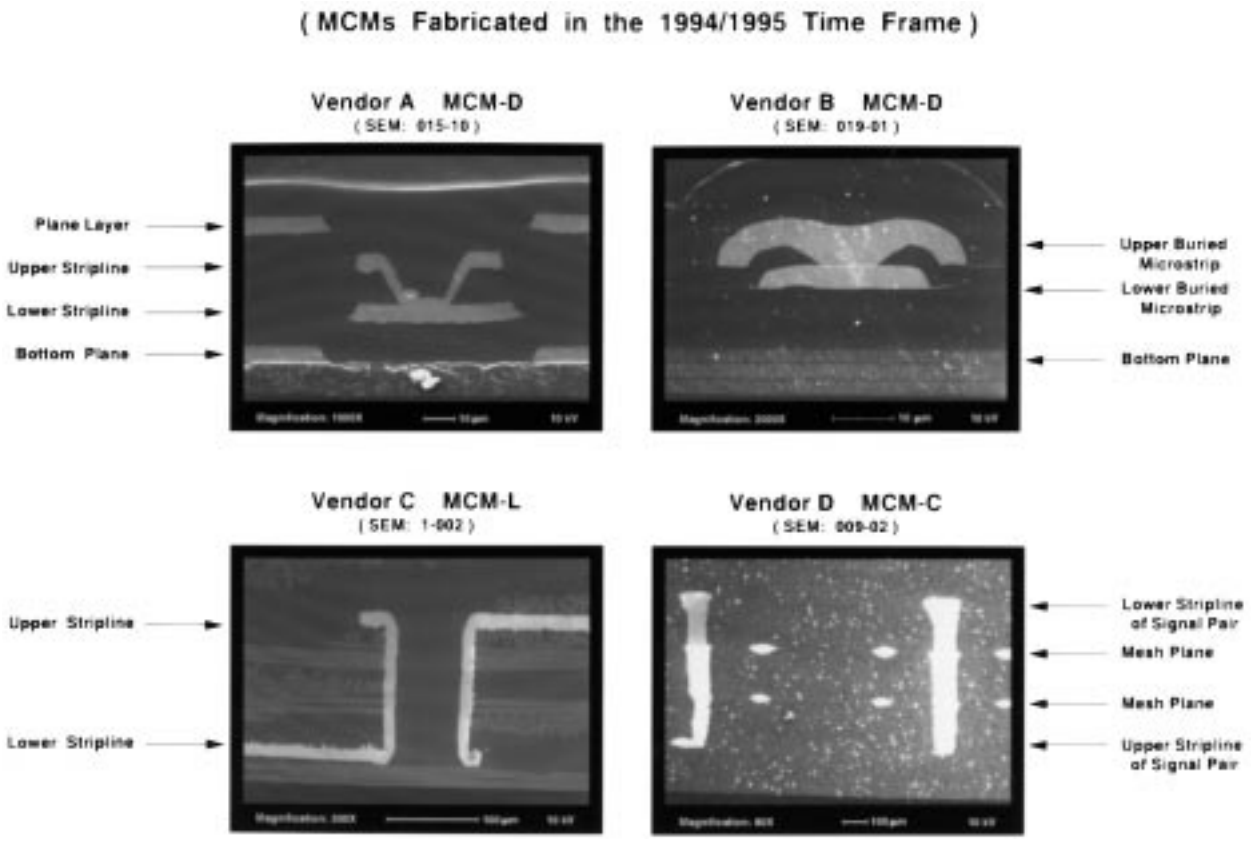

Fig. 7. Scanning electron micrographs of typical via structures in MCM-D's, MCM-L's, and MCM-C's manufactured with different fabrication recipes. Note the wide variety of substructural characteristics. Only Vendor D's vias resemble the typical post assumed in EM models of these substructures. (14522)

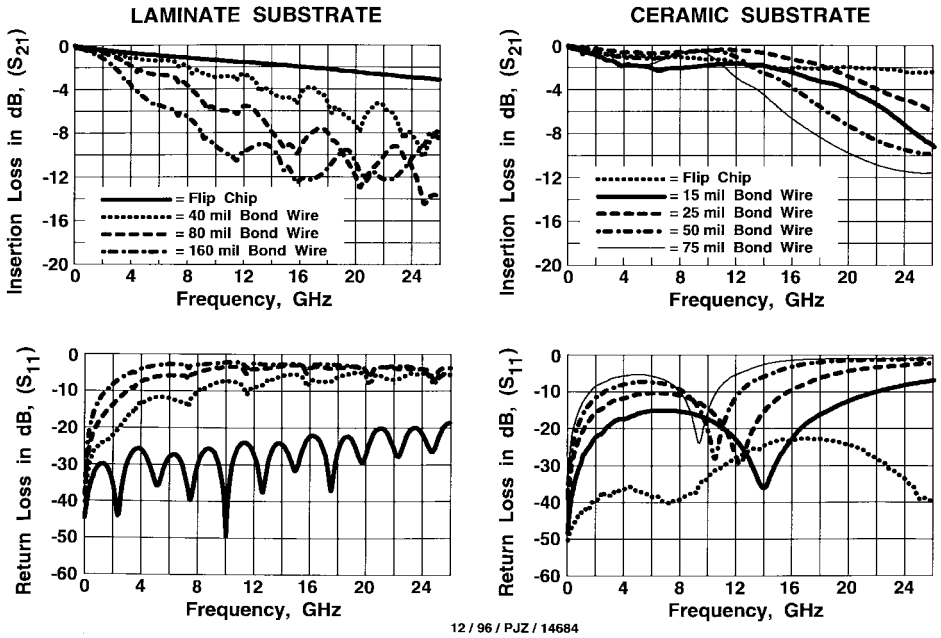

Fig. 8. Measured electrical performance of two methods of electrical contact, wire bonding and flip-chip attachment, between integrated circuits and either ceramic or laminate MCM's. In actual assemblies, 50-mil bond wires are the shortest practical lengths. Note degradation in insertion and return loss for even 40–50-mil bond wires in comparison to flip-chip contacts. (14684)

The incorporation of passive elements, i.e., R, L, and C components directly into the MCM substrates, is also a badly needed feature which is presently receiving much attention. Many systems targeted for MCM's consist of as much as 90% passive components. The six-channel global positioning system (GPS) receiver of Fig. 9 contains 150 components, of which only 11 are integrated circuits; the majority of the assembly cost was in the placement of the passives, which

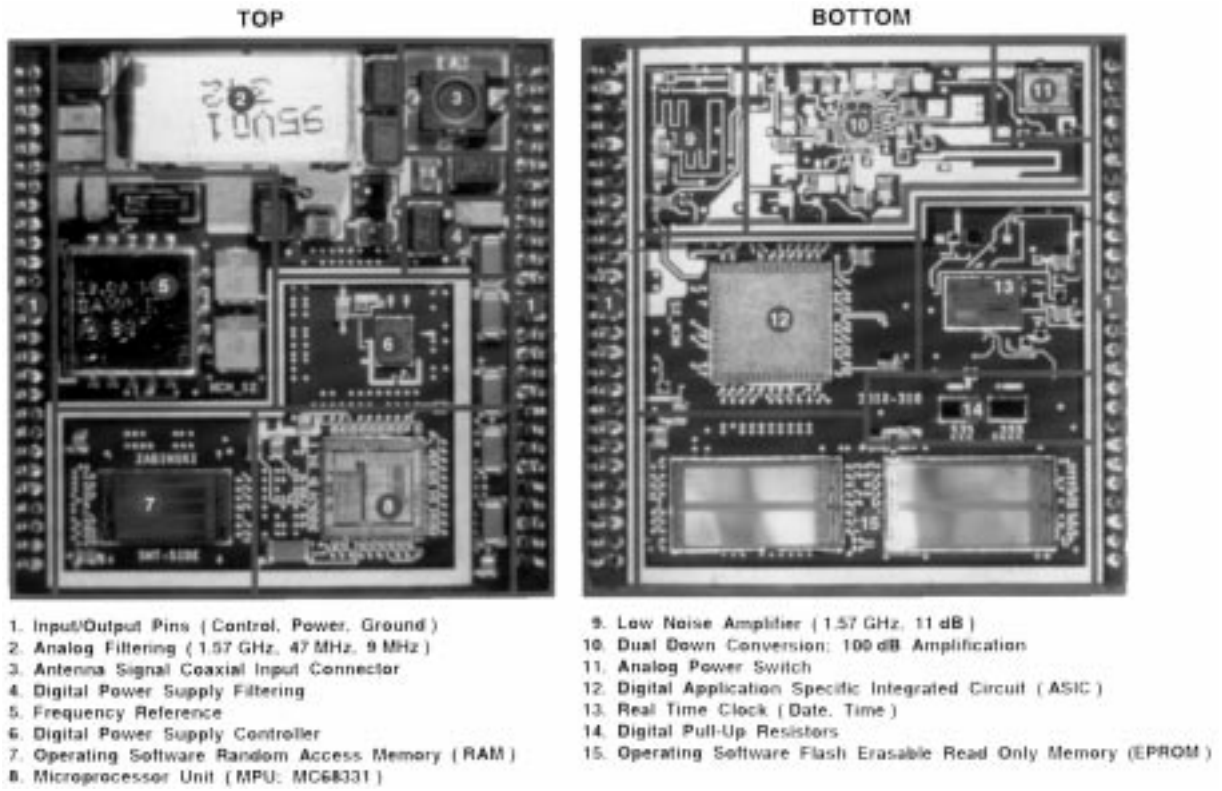

Fig. 9. Physical circuit functions of the top and bottom surfaces on microminiaturized GPS receiver fabricated on double-sided laminate MCM. Dimensions of MCM are 1.37 in $\times$ 1.43 in. Of the 150 components, 11 are integrated circuits and 139 are passive components. (12920)

consumed half the total real estate on this 1.37 in $\times$ 1.43 in MCM [8]. The substitution of **accurate** integral passive components for the discretes will have a major positive impact on cost and size of these modules.

V. How Can the Limitations of MCM Technology be Corrected?

Simulation studies conducted in our laboratory, discussions with numerous MCM fabricators, and some initial experiments in government-supported research laboratories indicate that most, if not all, of the deficiencies in the MCM technology cited above can be avoided through the application of improved and/or more accurate process steps.

Metal Deposition and Patterning, Dielectric Deposition, and In Situ Process Control

Figs. 6 and 7 illustrate the lack of control in the deposition of dielectric layers, and in the patterning of metal lines (i.e., the lack of control of the line cross sections) during the fabrication of all types of MCM's. Dielectric thickness control in MCM-L's appears problematic though not impossible, since the thickness of the cured laminate sublayers **and** the adhesive sublayers would both have to be under control. For organic and inorganic MCM-D's, dielectric thickness control is presently at $\pm$5–10 μm, whereas it should be at $\pm$1 μm. These levels of control are not unachievable. One manufacturer of fabrication equipment is developing a deposition coater for liquid-phase organic dielectrics with approximately $\pm$1-μm control, and has been reported to be achieving good initial success. For the inorganic dielectrics such as SiO_2, the same types of *in situ* process control which are beginning to appear in the integrated circuit manufacturing industry (but which are totally absent from the MCM fabrication industry) could be applied to control the deposition of inorganic dielectrics to less than $\pm$5% of the total dielectric thickness (i.e., the thickness tolerance of a 10-μm dielectric layer could be controlled to better than $\pm$0.5 μm). Initial studies recently conducted at a government-supported research fabrication facility appear to support this conclusion [9].

The fabrication of geometrically precise metal lines can likewise be brought under tight control. Presently in MCM-L's and MCM-D's, metal line definition is conducted through photopatterning followed by a wet-etch process, with either copper or aluminum as the conducting metal. The wet chemical processes are inexpensive, but lack tight geometric control (because (among other issues) of local differences in the concentration of the etchants within the baths, even with agitation, and the undercutting of the thin metal lines, which is typical of all wet-etch processes), a problem which was identified by the integrated circuit fabrication industry some years ago. This latter industry is turning increasingly to dry-etch processes such as reactive ion etching (RIE), which are slightly more expensive than wet-etch processes but can achieve much better control of the cross sections of interconnects. That the same types of processes can almost certainly be applied successfully to the fabrication of MCM's was recently demonstrated at a government-supported fabrication facility, which produced extremely rectangular line cross sections in 5 μm of aluminum [9], and the probability of maintaining similar control of line

cross sections with layers of aluminum up to 7–10 μm in thickness. Simulations in our laboratory indicate that these improved line structures on thicker dielectrics will exhibit 2–4 dB less loss (at all frequencies up to 10 GHz) on a 12-mm line than does the commercial version of this same process employing 2-μm thick lines.

Copper metallurgy, used since the early 1980s in many MCM's, typically relies on wet etching, or in some processes, sputter deposition and plateup to define the interconnect lines. These processes do not always exhibit maximum uniformity and repeatability batch-to-batch or even line-to-line. However, the integrated circuits industry is developing a highly precise interconnect process using copper rather than aluminum (the so-called copper damascene process, [10]), which may eventually apply to some inorganic MCM-D's as well. Though the bulk resistivity of copper is less than that of aluminum, it is the as-deposited resistivity of the metal, not its bulk value, which is relevant in the fabrication of MCMs; copper deposition and plating techniques typically yield only 80–85% of the bulk value of the metal.

Conversely, in the integrated circuit industry, aluminum is the most common interconnect metal. This industry has developed so-called hot-metal deposition techniques for aluminum, which result in sheet resistivities essentially the same as the bulk metal. Aluminum is also the metal most compatible with the dry-etch processes which have almost totally come to dominate the industry. If aluminum is more tractable and can be deposited in sufficient width and thickness to overcome its resistivity handicap, it should not be rejected out of hand. Electromigration of the aluminum should not be a problem in MCM's, because the current densities in the interconnects are much lower than in the chip interconnects. Conversely, the new interest in the integrated circuit industry in the damascene process [10] may indicate that the difficulties of working with copper may also eventually be overcome, and perhaps applied in the fabrication of even better MCM's. Furthermore, new approaches to the application of metal, such as chemical vapor deposition (CVD) of both aluminum and copper, presently being implemented in the integrated circuit industry, are also eventual candidates for use in MCM fabrication. Although the high-frequency electrical properties of these CVD-deposited metals are unknown at the present time, the nature of the CVD process should result in improved interconnect conductivity, in comparison to metal deposited by plating or sputtering.

Planarization and Increases in Layer Count

The MCM-L processes have an advantage over the MCM-D processes—since they are derivatives of the PWB technology, which assembles a stack of thin metal-covered dielectric laminate layers, the MCM-L processes can support a large number (at least 7–12) of metal layers. Some of the positive effect of this layer count is dissipated by the large vias which completely penetrate through the layer stack and compromise routing channels, but the layer count is irrefutably greater than with the MCM-D processes. The problem for the MCM-D technologies as presently implemented is that with the addition of each layer, an increasing loss of surface planarity occurs as the dielectric flows unevenly over the underlying metal structures. This same problem has been encountered in the integrated circuit industry, where the loss of planarity also limits the number of metal interconnect layers which can be achieved. Some sort of planarization is required to assure absolute surface flatness as a preparatory step for the deposition of the subsequent dielectric or metal layer, which will not only improve interconnect uniformity, but will also improve most via fabrication processes as well.

TABLE I
POSSIBLE APPROACHES TO ASSIGNMENT OF METAL LAYERS IN MULTICHIP MODULES. WITH ONLY ONE METAL LAYER, THE DESIGNER IS SEVERELY CONSTRAINED; WITH 7–8 LAYERS, CONSIDERABLE DESIGN FLEXIBILITY IS AVAILABLE. THE PHRASE "ROUTING/ATTACH" INDICATES THAT A SINGLE PHYSICAL METAL PLANE IS USED BOTH FOR ATTACHMENT PADS FOR CHIPS AND/OR PASSIVE COMPONENTS, AS WELL AS FOR MICROSTRIP INTERCONNECT (14376)

(Illustrative Implementations Only)

Number of Metal Layers	Design Restrictions	Suggested Layer Assignments
1		
2	Digital Systems Up to 25-50 MHz; Analog Microwave Designs Using Microstrip Interconnects with No Crossovers	1 Routing/Attach; 1 Shared Power/Ground Plane
3	Digital Systems Up to ~50 MHz with Split-Plane Power Delivery; Analog Microwave Designs Using Microstrip Interconnects	2 Routing; 1 Shared Power/Ground Plane
4	Digital Systems Up to ~1 GHz; Analog Microwave Systems Requiring Microstrip & Stripline Interconnect	2 Routing; 1 Power Plane; 1 Ground Plane
5	Digital Systems Up to ~2.5 GHz; Most Analog Microwave Systems	2 Routing; 1 Power Plane; 2 Ground Planes
6	Digital Systems up to 10-12 GHz; Analog Microwave Systems up to 12-15 GHz	2 Routing; 2 Power Planes; 2 Ground Planes
7	All Digital and All Analog or Mixed Signal Designs are Feasible	2 Routing; 1 Routing/Attach; 1 Power Plane; 2 Ground Planes; 1 Integrated Small Capacitor and/or Embedded Resistor Layer
8	All Digital and All Analog or Mixed Signal Designs are Feasible	2 Routing; 1 Routing/Attach; 2 Power Planes; 2 Ground Planes; 1 Integrated Small Capacitor and/or Embedded Resistor Layer

Routing = Signal Interconnect Layer
Attach = Component Attachment Layer

For the inorganic MCM-D's (upper right-hand panels of Figs. 6 and 7), chem–mechanical planarization (CMP) may be a useful approach [11]. CMP is presently being made cost effective for and by the integrated circuit industry, and there is reason to believe it could be made cost effective for the MCM industry as well. CMP is also known to be compatible with organic dielectrics, and is definitely worth pursuing. Improvements in layer-to-layer planarity should enable the incorporation of additional layers in all of the MCM-D processes, increasing the layer count from the now-common four layers to six or even eight layers. A proof of the feasibility of higher layer counts comes from one nonmerchant fabricator of organic MCM-D's, which has repeatedly demonstrated eight-layer MCM-D substrates; unfortunately, this capability is not available to the commercial marketplace. Table I illustrates the manner in which additional layers would be used by systems designers, if available.

Interconnects Between Layers of the MCM

As is apparent in Fig. 7, via fabrication remains a constraint on high frequency performance for most MCM processes. So-

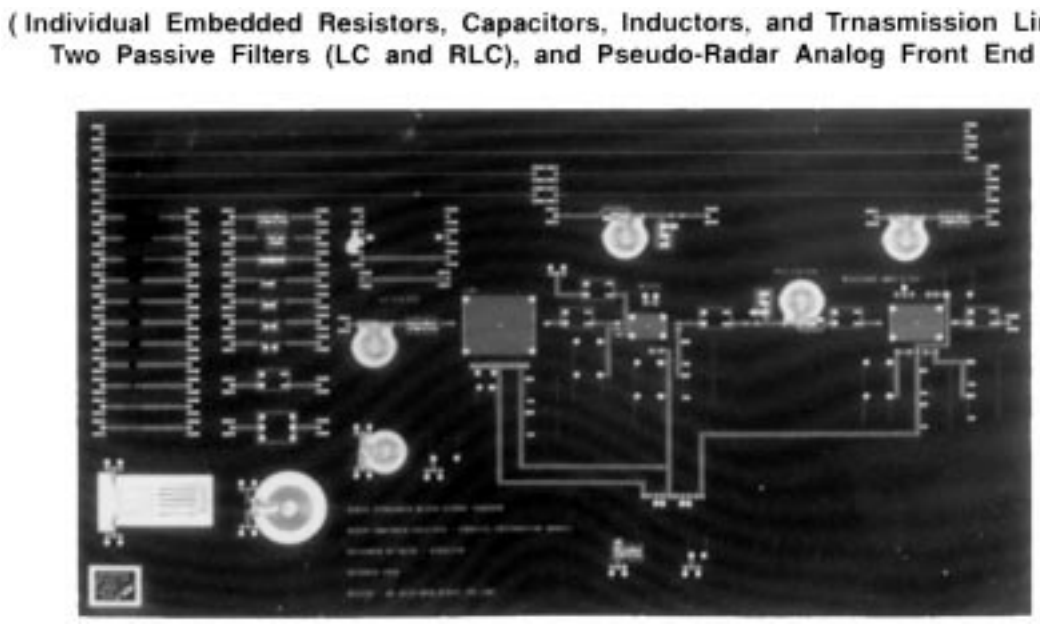

Fig. 10. Photo of experimental inorganic MCM-D containing a number of integrated passive elements. Note the integrated *LC* filter and the LNA, mixer, *RLC* filter, and wide-band amplifier in the right central portion of the MCM. This latter circuit represents a typical "front end" for a high-performance digital receiver. (14803)

called spiral staircase vias are used in most MCM processes because the lack of layer-to-layer planarity and the open nature of the via holes (with metallization only on their sloped sides) prevents placing vias penetrating single dielectric layers directly above one another; each single layer via must be offset from the one above and below by a small amount. The resultant spiral via structure is very lossy (particularly at high frequencies) and difficult to model accurately. Further, while the vias and associated capture pads of MCM-D's are no larger than the linewidths themselves, for MCM-L's and MCM-C's the vias are typically at least twice the width of the lines, while the capture pads are three times the linewidths. These outsized via structures create significant impedance discontinuities which degrade interconnect performance for frequency components greater than approximately 2–3 GHz. These via effects are *not* apparent in the right-hand "MCM-C" panels of Fig. 8, which employed simple microstrip lines without vias to allow the effects of the bond wires alone to be analyzed.

However, via structures can be improved. Solid post stacked vias have been demonstrated in some inorganic MCM-D and in MCM-C processes (lower right-hand panel of Fig. 7), and a stacked "coffee-cup" via approach is employed routinely in at least one organic MCM-D process. Further, smaller vias have been demonstrated in MCM-L's, though not yet in MCM-C's. Thus it is not impossible to produce vias penetrating multiple dielectric layers with good electrical performance. Designers and modelers must be aware of the limitations of the spiral and oversized vias, and must press the fabricators to improve via quality.

Development of Passive Components Integrated into MCM's

As illustrated in Fig. 9, many next-generation systems, particularly those containing both analog and digital components, will require large numbers (dozens to hundreds) of passive (R, L, and C) components for power plane decoupling and for elements of passive filters. The cost, surface area, and assembly yield impacts of employing discrete passive components are so unacceptable that much more work will be needed to assure the cost-effective integration of the passive elements directly into the MCM substrates during their fabrication. Although initial steps have been taken to develop such a capability and even to integrate complete passive filters directly into MCM substrates (as illustrated in Fig. 10), the integral components fabricated to date have manufacturing tolerances of $\pm 10\%$ for resistors, and $\pm 20\%$ or worse for capacitors and inductors.

These tolerances need to be improved to the range of $\pm 2\%$–5% for all three types of passive components (which also includes transformers as well as two-terminal inductors). The capacitors require exact definition of the plate areas, extremely accurate control of dielectric deposition, and accurate control of the permittivity (the "K" value or relative dielectric constant) of the dielectric material. The resistors require accurate deposition of the resistor material, in lateral extent, thickness, and sheet resistivity. The inductors require the ability to fabricate metal lines with good edge definition and significant metal thickness (up to 10 μm of metal thickness, more than is presently feasible). There is reason for optimism, since the same precision fabrication techniques which will improve line impedance tolerances can be applied to the accurate fabrication of integral passive components as well. These improvements should also encompass improved high-K and low-K dielectrics as well; though a separate discipline in itself, we consider the need for improved dielectrics to be intimately linked to the development of improved passives and have, therefore, included the requirement for improved dielectrics in the same "urgency category" as the components themselves. There is some reason for optimism,

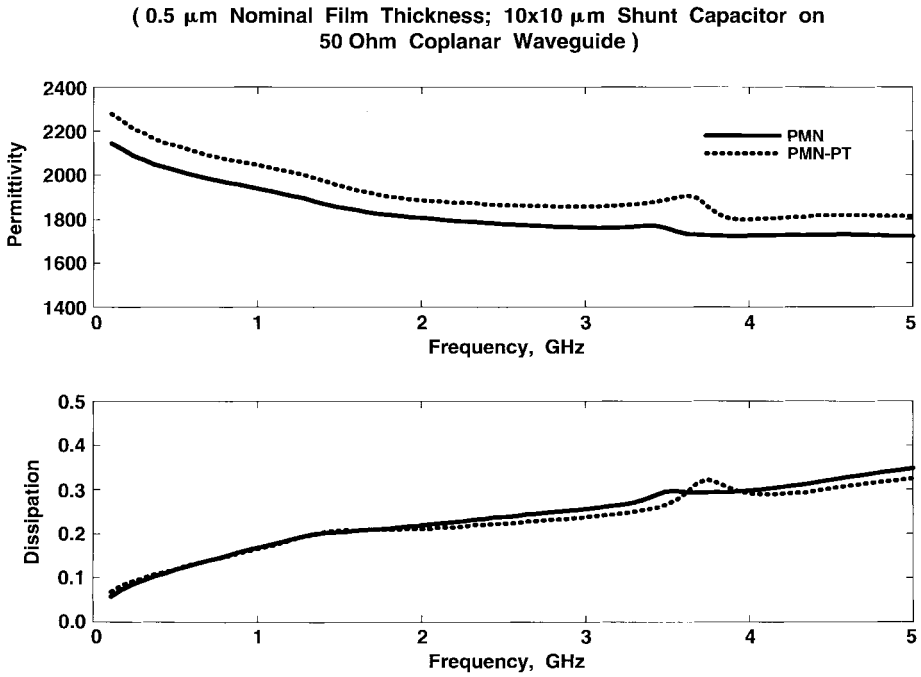

Fig. 11. Frequency dependent electrical properties of thin film high dielectric-constant (permittivity) lead manganese niobate material in two related forms. Thickness of the dielectric in these samples was approximately 0.5 μm. Note that the permittivity does not decrease up to 5 GHz, though the dissipation factor does increase at higher frequencies. The high dielectric constant values were observed to frequencies exceeding 10 GHz, and in many cases to 50 GHz. Dissipation factor can be traded off against dielectric constant by alterations in material formulation. (14338)

as several formulations of inorganic dielectrics show very high dielectric constants and acceptable dissipation factor well into the gigahertz frequency range (Fig. 11).

Flip-Chip Attachment or Chips-First Assembly

For analog microwave integrated circuits, or for digital components operating at clock rates above 500 MHz (one vendor of integrated circuits is actually delivering **microprocessors for the consumer market**, which operate at clock rates of 520 MHz!), the deleterious effects of wire bonds on electrical performance of interconnects (see Fig. 8) must be alleviated. The best approaches to this are the complete elimination of the wire bonds, either by embedding the chips in the substrate and passing all the interconnect over the tops of the chips and directly to the chip pads (referred to as a "chips-first" assembly process), or by flipping the chips over on a conventional MCM substrate and using reflowed solder-ball connections between the chip pads and matching pads on the MCM's. This process cannot be undertaken lightly; a chip contact pad intended for wire bonding is not quite the same as a pad intended for flip-chip attachment. In the latter case the (aluminum) chip-pad metallurgy may need to be altered to be compatible with the deposition of solder bumps, through the introduction of a barrier and adhesion layer between the aluminum and the solder material (aluminum will not wick solder). Further, the opening in the final passivation layer which exposes the metal of the pads may need to be of a different shape than for wire bonding, again to accommodate the deposition of the solder ball and its subsequent reflow. These issues can be accounted for easily by the chip designers if they are alerted ahead of time to the desire of the users to employ flip-chip attachment.

Another problem which has minimized the use of flip-chip attachment is that the developer of flip-chip methods—IBM—has traditionally spread their contact pads over the entire chip area ("area-array" pads). Unfortunately, a chip containing area-array pads cannot be wire bonded, since some bond wires would have to traverse half the width of the chip to reach internal pads. As a result, systems designers who must use a variety of components from many vendors have been reluctant to commit to area-array pads, since the option to wire bond is foreclosed on those chips. The IBM spacing rules and technology for area-array pads has been 8–10 mil, which, while fine for the area array, is too coarse if used as the pitch for peripheral pads for high pin count integrated circuits. Recently however, several large integrated circuit fabrication facilities have begun to develop the technology to support flip-chip attachment of chips with peripheral pads on a very tight 4.5–6-mil pitch. In such a case, a chip could be flip-chip attached or wire bonded at the discretion of the end user. Such changes will hopefully raise the acceptance level of flip-chip attachment, which in turn will improve the electrical behavior of the signal paths entering the highest performance integrated circuits. The MCM-D technology can easily handle these tight pitches, but the MCM-L and MCM-C technologies are not yet up to this challenge.

Thermomechanical Compatibility Issues

Next-generation integrated circuits will dissipate much more heat per unit area than at present. Even microprocessors for the consumer market are now dissipating as much as 30 W/cm^2; silicon components dissipating 150–200 W/cm^2 are on the horizon. Gallium arsenide (GaAs) A/D converter

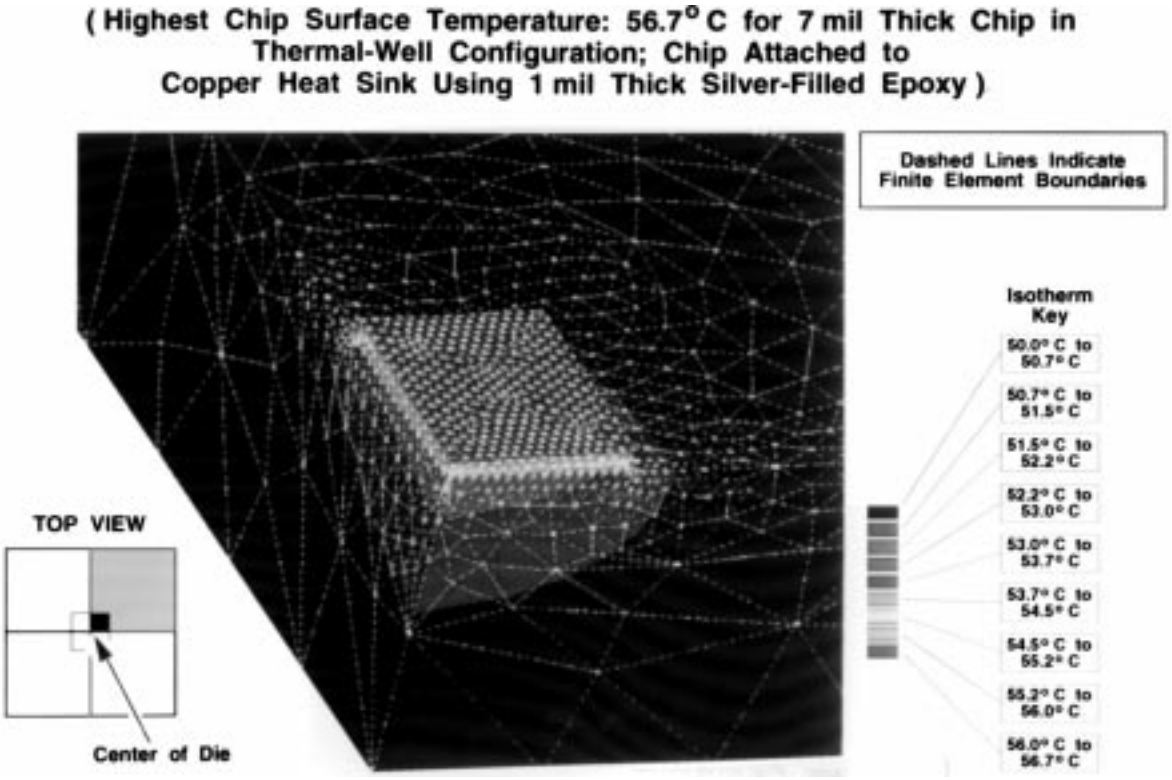

Fig. 12. ANSYS 3-D thermal model depicting isotherms resulting from GaAs die heat flux of 59 W/cm^2 with heat sink back side held at 50 °C. The die was thinned to 7 mil, and installed in a cavity in the MCM directly onto a copper heat stud. Note that chip temperature rise was constrained to 6.7 °C. (13354)

die are already dissipating 60 W/cm^2, which because of the lower thermal conductivity of GaAs, is equivalent to approximately 180–200 W/cm^2 in silicon. The removal of these high heat loads from sensitive high power density mixed-signal integrated circuits remains a difficult problem, which often must be addressed on a case-by-case basis. The three-dimensional (3-D) thermal model of Fig. 12 illustrates the maintenance of a small temperature rise in a 59-W/cm^2 GaAs A/D converter die using "heroic measures" including special thermal wells and exotic high conductivity substrate materials; however, these approaches are not presently cost effective except for the most expensive die. Better thermal treatments for MCM's, such as embedded layers of thin synthetic diamond, the use of aluminum nitride substrates, and the placement of die in wells directly on a cooling substrate, are being investigated and made more cost effective.

Further, because the thermal behavior of these die and their mechanical interaction with the host MCM are truly 3-D and time varying in nature (i.e., consisting of a transient component and a steady state component), the thermal modeling tools generally available from the computer aided design (CAD) vendors are inadequate to the task. Conversely, although finite-element analysis tools such as ANSYS developed for the aircraft industry are capable of conducting full 3-D time-varying thermomechanical transient and steady state analyses (as in Fig. 12), the use of these tools remains an art familiar to only a few engineers.

Development work will be required to yield new simulation methods with the power of the finite-element tools and the speed and user friendliness of the one-dimensional (1-D) and two-dimensional (2-D) approximation tools now offered by the major CAD vendors. The thermomechanical challenge includes an improved understanding of the effects of using so-called thermal underfill materials [12] between the chips and the MCM's when a flip-chip attachment method is employed; the exact thermomechanical behavior of the underfills (which are themselves still evolving) is still undergoing evolution.

Low-Volume Access to High-Volume Manufacturing Lines

The lack of low-volume access to high-volume production lines is perhaps the most vexing problem facing the U.S. DOD at present. This issue is more than just an economic one—it is temporal as well. A military system undergoes several stages of development lasting a number of years, during which only prototype quantities of modules are needed. When the system enters "production," the total fabrication run may number only in the low thousands, equivalent to 1–2 weeks of production for a high-volume commercial component (the **economic** aspect of the problem). Because MCM vendors cannot be expected to maintain a stable fabrication recipe over the five–ten year development cycle of a military system (the **temporal** problem), methods must be found **within the CAD systems** to modify designs to accommodate changes in fabrication recipes. One approach to this problem would be through an extension of the concept of "macros" used widely in the integrated circuit design environment: if via stacks, internal and peripheral pads, stripline and microstrip segments, passive components, etc., were treated thoroughly as library

elements, it might be possible to replace the macro libraries as the MCM technologies evolve, and essentially retarget the original MCM design to the new MCM technology. This is a problem (and a potential solution) which has not been addressed at all by the CAD tool vendors, but must be. It represents an area where vitally important research will be required to address the problem.

VI. Important Research Areas for the Modeling Community

Based on the observable trends in advanced system development, in the following subsections we describe fruitful areas for research which are seriously in need of exploration, and which are well suited for study by the simulation community. These areas will directly support the substrate and system development efforts described earlier in this paper.

Development of Rapidly Executing Truly 3-D Full Wave Electromagnetic Modeling Tools

A. Quasi-Static Algorithms

The simulation packages that have been most widely used to the present are based on quasi-static electromagnetic (EM) algorithms (QSA's). The principal mathematical underpinning supporting these packages is the Green's function integral-equation formulation for 2-D and 3-D multiconductor and multilayered transmission lines implemented with the method of moments (MOM), as originally proposed and amplified by Harrington *et al.* [13]–[14]. A number of refinements of, and modifications to, the MOM have been made, including the boundary-element method (BEM) [15], the singularity treatment [16], the spectral domain method [17], the even/odd basis function expansion [18], etc. In addition to the MOM approaches, the finite difference (FD) method [19] and the random walk method [20] have also been applied. Recently, a fast multipole method has been proposed [21], which may be a breakthrough for the computations of the capacitances of very large structures and systems based on the QSA's.

The standard static approaches can only obtain the distributed capacitances and external inductances of the transmission lines. The resistances and conductances are typically obtained based upon an assumption that the resistive and conductive losses are low [22]. The mathematical simplifications have made the quasi-static algorithms inaccurate, especially for very thin striplines, very lossy substrates (doped semiconductors), or at very high clock rates. It has been reported that the QSA's are valid only to 3–5 GHz for typical packaging structures. Mathematically, the quasi-static solution represents only a low frequency approximation to Maxwell's equations, and in fact, many high frequency phenomena, e.g., dispersion, radiation, transverse currents, longitudinal fields, etc. cannot be properly addressed by the QSA's. Either it will be necessary to develop extensions of the QSA's for higher frequencies, or research efforts will have to concentrate on truly full wave solutions.

B. Full-Wave Solutions

To model the EM performance of the packaging and interconnects with greater accuracy, more complicated formulations have been proposed, including the spectral domain method [23], [24], the Green's function approach [25], etc. For antenna and microwave problems, the metal patch width is always assumed to be much greater than the metal thickness. As a result, a "zero thickness assumption" can be used, and a Fourier transform in the direction perpendicular to the thickness direction can be employed, thereby simplifying the mathematical treatment significantly. Because of the narrow bandwidth of many antenna and microwave problems, and because the skin depth is usually much less than the metal thickness, an impedance boundary condition can be employed, once again greatly simplifying the modeling problem. In contrast, high clock rate digital circuits are typified by a wide signal spectrum, from nearly dc to many gigahertz. In addition, because the metal trace thickness in a typical MCM is on the order of 6–8 μm, it is not correct to assume that the line behavior is totally skin effect limited. In fact, some penetration of current into the inner regions of the conductor does occur, to such an extent that frequency-dependent internal inductance and resistance must also be accounted for.

To model the EM performance of the MCM's faithfully, comprehensive full wave analysis tools for complicated 3-D structures will definitely be required. The full wave methods may be classified into three groups as follows.

1) *The finite difference time domain (FDTD) method*: This class of techniques includes the FD method [26], [27] and its derivatives, the finite volume time domain (FVTD) method [28], and the finite difference frequency domain (FDFD) [29] method. It has been demonstrated [30] that the transmission line matrix (TLM) method is essentially equivalent to the FDTD method. Because of its mathematical simplicity and its flexibility in handling complex geometries, the FDTD method has been widely employed by the modeling and simulation community. In conjunction with absorbing boundary conditions (ABC's) and the concept of perfectly matched layers (PML's), the FDTD approach has been applied very successfully in computational EM's. The disadvantage of the FDTD is its requirements for very large amounts of local computer memory and large amounts of central processing unit (CPU) time. Recently, a wavelet based version of the FDTD has been proposed. For a rectangular cavity problem, the new method reduced the amount of local memory required to execute an example problem by a factor of 125 [31]. Considerably more research will be required to model conductors with finite conductivity and finite thickness. To improve the versatility of this method, nonuniform and nonorthogonal mesh structures need to be incorporated with the FDTD.
2) *The finite element method (FEM)*: A node based FEM has been used in EM modeling for decades. A problem associated with the FEM is its tendency to generate

spurious solutions [32]. Recently, new formulations of the edge based FEM, collectively referred to as the edge element method (EEM), have been developed [33], [34]. This new literature indicates that the spurious solutions ("modes") observed in the FEM are completely eliminated in the EEM. The EEM can handle conductors of finite conductivity and thickness very efficiently. The 2-D version of the EEM has sufficiently matured that a commercial package using this technique is now available. The large system of equations generated by the eigenvalue and eigenvector problems resulting from the EEM can be solved by the so-called "subspace iterative method" (also referred to as the Lanczos algorithm) to obtain the first few dominant modes. The EEM is also able to analyze structures of increased geometric complexity in comparison to the FEM approach. In combination with local radiation boundary conditions [35], and employing the so-called boundary conditions of the third kind [36], a large number of electrical packaging and EM compatibility/EM interference (EMC/EMI) problems (many of which have been under discussion in the literature for years [37], [38]), can be solved effectively. A Green's function is not even required for the EEM, which is a considerable advantage in comparison to the integral equation method (IEM).

3) *Integral equation method*: While the FDTD and FEM solve 3-D problems throughout the volume of interest (that is, a mesh is created throughout the 3-D space of interest), the IEM solves for the unknowns only on the boundary surfaces. For a physical problem with a linear dimension of n intervals, the number of unknowns for the FDTD and FEM is proportional to n^3, while for the IEM the number of unknowns is proportional to n^2. In comparison to the FEM, the IEM appears to be much more computationally efficient. However, the corresponding FEM matrix is sparse, while the IEM matrix is dense.

Recent attempts have been made to incorporate the results from wavelet theory into the IEM [39]. Due to the multiresolution analysis (MRA) features of wavelets, very sparse matrices have been obtained with the IEM. Mathematicians have proved that the nonzero elements in the resultant impedance matrix are proportional to n [40], rather than to n^2. Despite the considerable potential of this combined technique, some workers have claimed that the advantage of achieving sparse matrices is outweighted by the complexity and "overhead" of the wavelet method. The apparent reason for this expressed concern is that most of the wavelets do not have closed form expressions, which makes the evaluation of the matrix elements (usually through Gaussian quadrature) more difficult. The authors of [40] have demonstrated that by using Coifman wavelets (which have zero moments for both the father and mother wavelets), the computation of the matrix elements can even be faster than the co-location method (pulse basis and Dirac-delta testing functions) [41]. Although a number of issues remain to be addressed, the entire class of wavelet methods appears to represent a very powerful set of techniques worthy of further investigation.

In summary, it seems clear that fast, accurate, and more effective simulation tools using state-of-the-art theory and techniques need to be developed which will model 3-D structures efficiently. A combined FEM/IEM method employing newly emerging fast computational methods, e.g., wavelets or fast multipole approaches, appear to show the most promise.

Tools for Analysis of EMC/EMI Problems

Concerns regarding EMC/EMI have been raised in recent years, and the problems have escalated as system clock rates continue to increase and the integration density of VLSI circuits dramatically increases. Thus far, only very simple models of the EMC/EMI problem have been proposed. The conduction and radiation emission and susceptibility models that have appeared in the recent literature remain far below the complexity of real-world problems. These models are still at the component level, while the FCC/CISPR standards have been established at the system or subsystem levels. The amount of EMI generated by a digital processor is directly related to the edge rates of the signals, the system clock rate, the total amount of switching current, and the size and shielding effectiveness of the device or system [37], [38]. Due to the enormous complexity of an actual processor system, it is likely that a combined deterministic and statistical approach may be necessary to address these problems.

Improved Understanding of Power/Ground Plane Systems in PWB's and MCM's

For decades there has been widespread confusion and uncertainty regarding even the most generic high frequency behavior of power/ground plane delivery systems. Generations of engineers have applied *ad hoc* design rules to the decoupling of power and ground supplies from one another and the suppression of noise on these planes, such as: "Install one decoupling capacitor (two capacitors? three capacitors?) on the circuit board or MCM for each integrated circuit (for every three integrated circuits? for every power pin?)." These rules have become "lore" based upon individual successes, but have had no theoretical underpinning.

The past several years have witnessed remarkable theoretical progress in developing a comprehensive understanding of these important substructures [42]–[47]. It is beginning to appear that the "noise" on these planes is by no means a set of random fluctuations caused directly by the state switching of the digital chips. Rather, the "noise" is actually a complex resonant behavior of an essentially high Q circuit with a very large number of resonant modes, which are in turn "pumped" by harmonic components in the state switching currents of the integrated circuits.

Because many of the proposed next-generation analog- or mixed-signal systems have already been demonstrated to be exceptionally sensitive to disturbances on their power and ground planes [7], these resonances must be made amenable to complete characterization. Further, suppression of the resonant modes, at least within the signal passbands of interest [44] (especially in the development of all-digital receivers) will be mandatory. Much more work will be required to understand

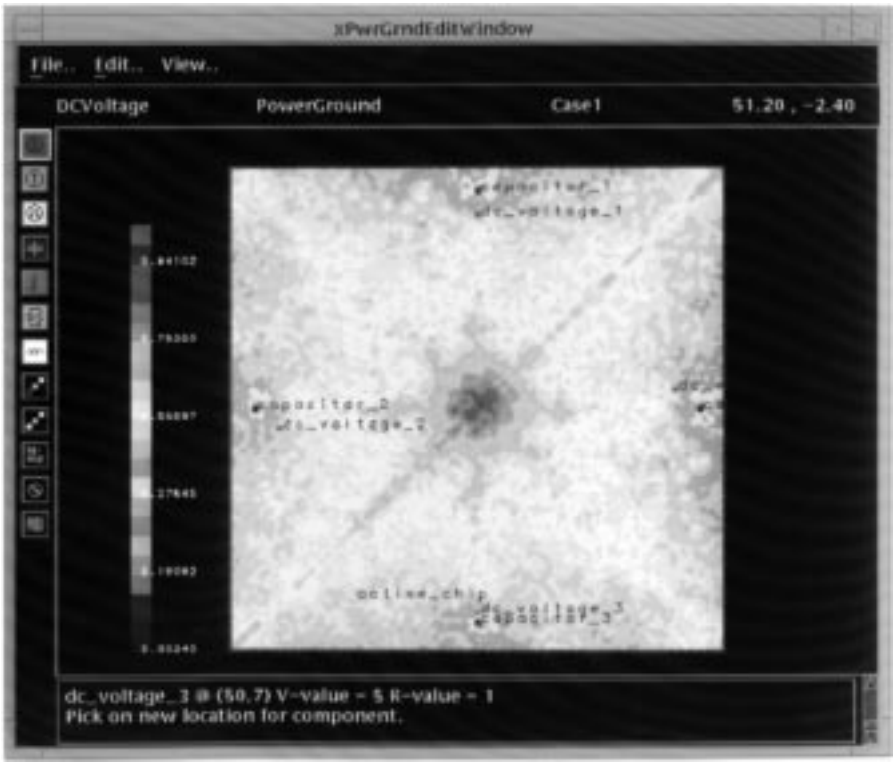

Fig. 13. Noise surface display of disturbances in the power/ground plane sandwich of a typical MCM 0.5-in square. Note the distinct patterned behavior of the peak-to-peak disturbances, illustrating that power/ground plane "noise" is actually a complex but repeatable phenomenon which can be understood and dealt with within the context of high-Q resonant circuits. (14647)

these phenomena in both the time and frequency domains; thereafter, the design community will need numerically robust CAD tools with user-friendly interfaces understandable by engineers without deep theoretical understanding of the underlying phenomena. Fig. 13, a "noise surface" of a small MCM exposed to a periodic disturbance, is a feasibility demonstration that such CAD tools, supported by a theoretical understanding of the underlying phenomena, are feasible.

Improved 3-D Thermomechanical Modeling Tools

Cooling methods must be developed to handle the increasing power-dissipation levels which have occurred over the past few generations of processors, and which, as indicated earlier, give every indication of continuing to increase. These heat removal methods must be cost effective, manufacturable, and easily integrable into the server, desktop, special purpose signal processor, and wireless/mobile markets. Critical areas for research concentration include advanced materials with excellent thermal properties which will aid in heat removal, and a thorough understanding of integration and manufacturability constraints. Package design techniques will be needed, which account for mismatches in coefficients of thermal expansion (CTE), especially transient CTE mismatches. The design of packages which can support area array contacts on large integrated circuits, and the techniques to assemble area array chips onto the MCM's, must be understood for the newly emerging organic materials which are being applied to electronic packaging. Thermomechanical modeling research needs to concentrate on the identification of basic failure mechanisms, lifetime prediction models, and the development of improved modeling tools. Although at present the finite element-based tools are widely used for this type of modeling, in the future, nonlinear programming-based design optimization methodologies may be employed to evaluate and improve existing electronic packages. Finally, an approach which combines CAD tools with experimentally driven prototype verification may need to be fully developed.

VII. Conclusions

In this paper, we have reviewed the manner in which electronic packaging will be driven by the high level performance requirements of next-generation mixed-signal systems and by the evolving characteristics of next-generation integrated circuits. Present performance and fabrication limitations of the MCM technology have been described, as well as possible approaches to remove or minimize these constraints. It appears that military applications will be more technically challenging, but that the volumes of product required by the DOD will be overwhelmed in the near term by less demanding, but much higher volume, commercial and consumer applications. Areas fruitful for research by the simulation community have also been elucidated. It is hoped that this review will provide a broad applications-oriented framework for the theoretical and simulation-directed papers in this special issue on interconnect and packaging.

Acknowledgment

The authors wish to thank G. Fokken, M. Lorsung, D. Schwab, and P. Zabinski of Mayo Foundation, Rochester,

MN, D. Shaver, and C. Keast of MIT Lincoln Laboratories, Boston, MA, J. Murphy and Z. Lemnios of DARPA/ETO, C. Hanson, NRaD Code 80, for support and helpful discussions, and S. Richardson, E. Doherty, D. Jensen, and L. Mason of Mayo Foundation, for preparation of text and figures.

REFERENCES

[1] P. J. Zabinski, B. K. Gilbert, P. J. Zucarelli, D. V. Weninger, and T. W. Keller, "Example of a mixed-signal global positioning system (GPS) receiver using MCM-L packaging," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 18, pp. 13–17, Feb. 1995.

[2] M. J. Ellsworth, H. Hamel, E. D. Perfecto, and T. Wassick, "A high density, high performance MCM-D/C package: A design, electrical, and process perspective," in *Proc. Electron. Comp. Technol. Conf.*, 1996, pp. 821–828.

[3] B. K. Gilbert, B. A. Randall, B. L. Donham, D. J. Schwab, D. C. Benson, D. B. Tuckerman, and W. P. Goodwin, "Implementation of a gallium arsenide multichip digital circuit operating at 500–1000 MHz clock rates using a Si/Cu/SiO_2, MCM-D technology," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 20, pp. 17–26, Feb. 1997.

[4] T. M. Schaefer, J. J. Kacines, B. A. Randall, L. E. Roszel, G. J. Fokken, D. Walter, D. J. Schwab, L. Mowatt, and B. K. Gilbert, "A chips-first multi-chip module implementation of passive and active test coupons utilizing Texas instruments high density interconnect technology," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 19, pp. 403–416, May 1996.

[5] T. R. Haller, B. S. Whitmore, P. J. Zabinski, and B. K. Gilbert, "High frequency performance of GE high density interconnect modules," *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 16, pp. 21–27, Feb. 1993

[6] B. A. Randall, D. J. Schwab, D. C. Benson, J. L. F. Goldstein, R. Zenner, J. H. Burkhardt, and B. K. Gilbert, "GaAs digital MCM implemented in Si/Cu/SiO_2 technology with flip chip attachment for clock rates up to 1 GHz," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, to be published.

[7] R. L. Thompson, M. J. Degerstrom, E. L. H. Amundsen, P. J. Riemer, M. E. Vickberg, and B. K. Gilbert, "An 8-bit 2.5 gigasample A/D converter multichip module for all-digital radar receiver for AN/APS 145 radar on Navy E2-C Airborne Early Warning Aircraft," presented at the *IEEE Multi-Chip Module Conf.*, Santa Cruz, CA, Feb. 4–5, 1997.

[8] P. J. Zabinski, M. E. Vickberg, B. K. Gilbert, P. J. Zucarelli, D. V. Weninger, T. W. Keller, and D. M. Yee, "Case study, the design of a mixed-signal global positioning system receiver using multichip module packaging," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 19, pp. 215–224, Feb. 1996.

[9] C. Keast, MIT Lincoln Laboratories, unpublished.

[10] C. A. Nichols, S. M. Rossnagel, and S. Hamaguchi, "Ionized physical vapor deposition of Cu for high aspect ratio damascene trench fill applications," *J. Vacuum Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 14, no. 5, pp. 3270–3275, Sept./Oct. 1996.

[11] R. Telfeyan, J. Moyne, N. Chaudhry, J. Pugmire, S. Shellman, D. Boning, W. Moyne, A. Hurwitz, and J. Taylor, "A multilevel approach to the control of a chemical-mechanical planarization process," *J. Vacuum Sci. Technol. A, Surf. Films*, vol. 14, no. 3, pp. 1907–1913, May/June 1996.

[12] S. Rzepka and M. Ekkehard, "Flip chips directly attached to FR4 printed circuit boards: FEM simulations and experimental tests," in *Proc. Flip Chip, BGA, TAB, and AP Symp.*, 1995, pp. 9–15.

[13] C. Wei, R. Harrington, J. Mautz, and T. Sarkar, "Multiconductor transmission lines in multilayered dielectric media," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 439–449, Apr. 1984.

[14] S. Rao, T. Sarkar, and R. Harrington, "The electrostatic field of conductor bodies in multiple dielectric media," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 1441–1448, Nov. 1984.

[15] G.-W. Pan, G. Wang, and B. Gilbert, "Edge effect enforced boundary element analysis of multilayered transmission lines," *IEEE Trans. Circuits Syst. I*, vol. 39, pp. 955–963, Nov. 1992.

[16] H. Igarashi, Y. Mizuyama, and T. Honma, "A boundary element analysis of transmission-line parameters using singular elements," *IEEE Trans. Magn.*, vol. 32, pp. 686–689, May 1996.

[17] W. Delbare and D. Dezutter, "Space-domain Green's function approach to the capacitance calculation of multiconductor lines in multilayered dielectrics with improved surface charge modeling," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1562–1568, Oct. 1989.

[18] G. Matthaei, G. Chinn, C. Plott, and N. Dagli, "A simplified means for computation of interconnect distributed capacitances and inductances," *IEEE Trans. Computer-Aided Design*, vol. 11, pp. 513–524, Apr. 1992.

[19] C. Taylor, G. Elkhouri, and T. Wade, "On the parasitic capacitances of multilevel parallel metallization lines," *IEEE Trans. Electron Devices*, vol. 32, pp. 2408–2414, Nov. 1995.

[20] Y. Coz and R. Iverson, "A high-speed multi-dielectric capacitance-extraction algorithm for MCM interconnects," in *Proc. IEEE Multi-Chip Module Conf.*, Santa Cruz, CA, Mar. 18–20, 1992, pp. 86–89.

[21] K. Nabor, S. Kim, and J. White, "Fast capacitance extraction of general three-dimensional structures," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 1496–1506, July 1992.

[22] M. AbuShaaban and S. Scanlan, "Modal circuit decomposition of lossy multiconductor transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 1046–1056, July 1996.

[23] R. Mittra and T. Itoh, "A new technique for the analysis of the dispersion characteristics of microstrip lines," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, pp. 47–55, Jan. 1971.

[24] V. Tripathi and H. Lee, "Spectral domain computation of characteristic impedances and multiport parameters of multiple coupled microstrip lines," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 215–221, Jan. 1989.

[25] R. Jackson and D. Pozar, "Full-wave analysis of microstrip open-end and gap discontinuities," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 1036–1042, Oct. 1985.

[26] K. Yee, "Numerical solution of initial boundary value problems involving Maxwell's equations in isotropic media," *IEEE Trans. Antennas Propagat.*, vol. 14, pp. 302–307, May 1966.

[27] A. Taflov and K. Umashankar, "Review of FDTD numerical modeling of EM wave scattering and radar cross section," in *Proc. IEEE*, vol. 77, pp. 682–699, May 1989.

[28] K. Huh, M. Shu, and R. Agarwal, "A compact high-order finite volume-time domain/frequency-domain method for electromagnetic scattering," presented at the *AIAA Conf.*, Jan. 6–9, 1992, Reno, NV.

[29] R. Holland, V. Cable, and L. Wilson, "Finite-volume time-domain (FVTD) techniques for EM scattering," *IEEE Trans. Electromag. Compat.*, vol. 33, pp. 281–294, Nov. 1991.

[30] W. Hoefer, "The transmission-line matrix method—Theory and applications," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 882–893, Oct. 1985.

[31] M. Krumpholz and L. Katehi, "MRTD: New time-domain schemes based on multiresolution analysis," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 555–571, Apr. 1996.

[32] G. Slade and K. Webb, "Computation of characteristic impedance for multiple microstrip transmission lines using a vector finite element method," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 34–40, Jan. 1992.

[33] J. Lee, D. Sun, and Z. Cendes, "Full-wave analysis of dielectric waveguides using tangential vector finite elements," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 1262–1271, Aug. 1991.

[34] J. Tan and G. Pan, "A new edge element analysis of dispersive waveguiding structures," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 2600–2607, Nov. 1995.

[35] A. Peterson, "Vector finite element formulation for scattering from two-dimensional heterogeneous bodies," *IEEE Trans. Antennas Propagat.*, vol. 43, pp. 357–365, Mar. 1994.

[36] J. Jin, *The Finite Element Method in Electromagnetics*. New York: Wiley, 1993.

[37] R. Sorrentino and S. Pileri, "Method of analysis of planar networks including radiation loss," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, pp. 942–948, Sept. 1981.

[38] R. B. Schulz, V. C. Plantz, and D. R. Brush, "Shielding theory and practice," *IEEE Trans. Electromag. Compat.*, vol. 30, pp. 187–201, Aug. 1988.

[39] G. Beylkin, R. Coifman, and V. Rokhlin, "Wavelets in numerical analysis," in *Communications on Pure and Applied Mathematics XLIV*. Easton, MD, Waverles Press, 1991, pp. 141–183.

[40] I. Daubechies, *Ten Lectures on Wavelets* (CBMS-NSF Applied Mathematics Series). SIAM, 1991.

[41] G.-W. Pan, J. Du, M. Toupikov, and B. Gilbert, "Application of intervallic wavelets to the surface integral equations," presented at the *IEE Proc. Microwaves, Antennas, Propagat.*, June 1995.

[42] G.-T. Lei, R. W. Techentin, P. R. Hayes, D. J. Schwab, and B. K. Gilbert, "Wave model solution to the ground/power plane noise problem," *IEEE Trans. Instrum. Meas.*, vol. 44, pp. 300–303, Apr. 1995.

[43] G.-T. Lei, G.-W. Pan, and B. K. Gilbert, "Examination, clarification, and simplification of modal decoupling method for multiconductor

transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 2090–2100, Sept. 1995.
[44] ———, "Power distribution noise suppression using transmission line termination techniques," in *Proc. 5th Topical Meeting Elect. Performance Electron. Packaging*, Napa, CA, 1996, Oct. 28–30.
[45] R. Mittra, S. Chebolu, and W. D. Becker, "Efficient modeling of power planes in computer packages using the finite difference time domain method," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1791–1795, Sept. 1994.
[46] D. A. Seeker and J. L. Prince, "Effects and modeling of simultaneous switching noise for BiCMOS off-chip drivers," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 19, pp. 473–480, Aug. 1996.
[47] J. Fang, Z. Chen, and Y. Chen, "Reduction of power and ground noise coupling in mixed signal modules," in *Proc. Symp. Elect. Performance Electron. Packaging*, Napa, CA, Nov. 1996, pp. 90–92.

Barry K. Gilbert (S'62–M'70–SM'87) received the B.S. degree in electrical engineering from Purdue University, West Lafayette, IN, in 1965, and the Ph.D. degree in physiology and biophysics with minors in electrical engineering and applied mathematics from the University of Minnesota at Minneapolis St. Paul, in 1972.

He is currently a Staff Scientist in the Department of Physiology and Biophysics, and the Director of the Special-Purpose Processor Development Group, Mayo Foundation, Rochester, MN. His research interests include the development of algorithms for the real-time transmission and analysis of wide-bandwidth image and signal data, the design of specialized signal-processing computers to execute these tasks, the development of CAD tools to allow the timely design of high-complexity digital-signal processors, the advancement of high-performance integrated-circuit technologies, such as gallium arsenide and indium phosphide, which can be used to assemble very high-performance signal processors, and the development of advanced electronic packaging technologies such as MCM's, which will be capable of supporting digital integrated-circuit-based processors operating at gigahertz system clock rates.

Guang-Wen (George) Pan (S'81–M'84–SM'94) received the M.S. and Ph.D. degrees in electrical engineering from the University of Kansas, Lawrence, in 1982 and 1984, respectively.

From 1984 to 1985, he was a Post-Doctoral Fellow at the University of Texas at Arlington. In 1985, he joined the Mayo Foundation, where he worked on the theory for the EM modeling of packaging and interconnections for high-speed integrated circuits and printed circuit boards. From 1986 to 1988, he was an Associate Professor of electrical engineering at South Dakota State University. From 1988 to 1993, he was an Associate Professor, Department of Electrical Engineering and Computer Science, University of Wisconsin–Milwaukee, and became a Professor in 1993. Since 1995, he has been Professor and Director of the Electronic Packaging Laboratory, Department of Electrical Engineering, Arizona State University, Tempe. His interests are the modeling of high-frequency and wideband signal-propagation phenomena in high-performance integrated circuits, MCM's, and printed circuit boards, and in the design of high-performance antennas for a variety of applications.